Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore
Shri Vaishnav Institute of Technology and Science
Choice Based Credit System (CBCS) in the Light of NEP-2020
M. Tech. (VLSI Design)
(2025-2027)

COURSE CODE	CATEGORY	COURSE NAME	TEACHING &EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
MTVD113		VLSI Technology	60	20	20	-	-	3	0	0	3

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; **C** - Credit;
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Course Educational Objectives (CEOs):

This course aims to:

1. Understand the fundamentals of semiconductor wafer preparation and cleanroom practices.
2. Learn key fabrication processes like oxidation, lithography, doping, and deposition.
3. Apply process knowledge to analyze and compare semiconductor fabrication techniques.
4. Build a foundation for advanced studies in VLSI, devices, and nanotechnology.

Course Outcomes (COs):

After successfully completing the course students will be able to:

1. Describe wafer preparation and cleanroom requirements.
2. Explain oxidation processes and kinetics.
3. Elaborate lithography and photoresist techniques.
4. Compare diffusion and ion implantation for doping.
5. Explain deposition methods and applications.

Syllabus:

Unit I: Overview of Semiconductor Processing **8 Hrs**

Electronic grade silicon preparation, Crystal growth, Czochralski process, Wafer-preparation, Slicing, Marking, Polishing, Evaluation. Basic wafer fabrication operations, Wafer sort, Clean-room construction and maintenance.

Unit II: Oxidation **7 Hrs.**

Objectives, Silicon dioxide layer uses, Thermal oxidation mechanism and methods, Kinetics of oxidation, Deal Grove model, Oxidation processes, Post oxidation evaluation.

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Unit III: Basic Patterning **8 Hrs**

Overview of Photo masking process, Ten step process, Basic photoresist chemistry, Comparison of positive and negative photoresists, X-ray lithography, Electron beam exposure system.

Unit IV: Doping **9 Hrs**

Definition of a junction, Formation of doped region and junction by diffusion, Diffusion process steps, Deposition, Drive-in-oxidation, Ion implantation- concept and system, implant damage, Comparison of diffusion and ion-implantation techniques.

Unit V: Deposition **9 Hrs**

Chemical Vapor Deposition (CVD), CVD Process steps, CVD System types, Low Pressure CVD (LPCVD), Plasma-enhanced CVD (PECVD), Vapor Phase Epitaxy (VPE), Molecular Beam Epitaxy (MBE), SOS (Silicon on Sapphire) and SOI (Silicon on Insulator), Introduction to Metaliization.

Textbooks:

1. S. M. Sze, VLSI Technology, McGraw-Hill.
2. S. K. Gandhi, VLSI Fabrication Principles: Silicon and Gallium Arsenide, Wiley.
3. Peter Van Zant, Microchip Fabrication: A Practical Guide to Semiconductor Processing, McGraw-Hill.
4. S. O. Kasap, Principles of Electronic Materials and Devices, McGraw-Hill.

References:

1. D. Nagchoudhuri, Basic VLSI Design and Technology, PHI.
2. B. G. Streetman and S. Banerjee, Solid State Electronic Devices, Prentice Hall.
3. S. Grove, Physics and Technology of Semiconductor Devices, Wiley.

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Choice Based Credit System (CBCS) in Light of NEP-2020
MBA+Ph.D. - III SEMESTER (2022-2024)

MBAI301C ADVANCEDHUMAN VALUES AND PROFESSIONAL ETHICS

COURSE CODE	CATEGORY	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
MBAI301C	AECC	Advanced Human Values and Professional Ethics	60	20	20	-	-	3	-	-	3

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical: **C** - Credit; **AECC**- Ability Enhancement Compulsory Course

***Teacher Assessment** shall be based on following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Objective

The objective of the course is to disseminate the theory and practice of moral code of conduct and familiarize the students with the concepts of "right" and "good" in individual, social and professional context

Examination Scheme

The internal assessment of the students' performance will be done out of 40 Marks. The semester Examination will be worth 60 Marks. The question paper and semester exam will consist of two sections A and B. Section A will carry 36 Marks and consist of five questions, out of which student will be required to attempt any three questions. Section B will comprise of one or more cases / problems worth 24 marks.

Course Outcomes

1. Help the students to understand right conduct in life.
2. To equip students with understanding of the ethical philosophies, principles, models that directly and indirectly affect personal and professional life.

COURSE CONTENT

Unit I: Inculcating Values at Workplace

1. Values: Concept, Sources, Essence
2. Classification of Values.
3. Values in Indian Culture and Management: Four False Views, Value Tree
4. Eastern and Western Values; Values for Global Managers

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MBA+Ph.D. - III SEMESTER (2022-2024)

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MBAI301C	AECC	Advanced Human Values and Professional Ethics	60	20	20	-	-	3	-	-	3

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical: **C** - Credit; **AECC**- Ability Enhancement Compulsory Course

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Unit II: Professional Ethics

1. Ethics: Concept, Five P's of Ethical Power, Organisational Tools to Cultivate Ethics
2. Theories of Ethics: Teleological and Deontological
3. Benefits of Managing Ethics in an Organisation
4. Ethical Leadership

Unit III: Indian Ethos and Management Style

1. Indian Ethos and Workplace
2. Emerging Managerial Practices
3. Ethical Considerations in Decision Making and Indian Management Model
4. Core Strategies in Indian Wisdom and Ethical Constraints

Unit IV: Human Behavior – Indian Thoughts

1. Guna Theory
2. Sanskara Theory
3. Nishkama Karma
4. Yoga: Types, Gains; Stress and Yoga

Unit V: Spirituality and Corporate World

1. Spirituality: Concept, Paths to Spirituality
2. Instruments to achieve spirituality
3. Vedantic Approach to Spiritual and Ethical Development
4. Indian Spiritual Tradition.

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MBA+Ph.D. - III SEMESTER (2022-2024)

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MBAI301C	AECC	**Advanced Human Values and Professional Ethics**	60	20	20	-	-	3	-	-	3

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical: **C** - Credit; **AECC**- Ability Enhancement Compulsory Course

***Teacher Assessment** shall be based on following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Suggested Readings

1. Kausahl, Shyam L. (2006). ***Business Ethics – Concepts, Crisis and Solutions***. New Delhi: Deep and Deep Publications Pvt. Limited
2. Murthy, C.S.V. (2012). ***Business Ethics –Text and Cases.*** Himalaya Publishing House: Mumbai
3. Chakraborty, S. K. (1999). ***Values and Ethics for Organizations***. Oxford university press
4. D.Senthil Kumar and A. SenthilRajan (2008). ***Business Ethics and Values.*** Himalaya Publishing House: Mumbai

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Master of Technology

SEMESTER I

COURSE CODE	Category	COURSE NAME	TEACHING & EVALUATION SCHEME								
			THEORY			PRACTICAL		Th	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
MTMAN 101	BS	Advanced Mathematics	60	20	20	-	-	3	0	0	3

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Course Educational Objectives (CEOs):

To introduce the students to advanced mathematics.

Course Outcomes (COs):

After the successful completion of this course students will be able to:

A. understand the concept of a vector space, subspace, basis, dimensions and their properties.
B. find solution/numerical solution of PDE.
C. explain fundamental principles of probability theory.
D. understand the concept of Markov process and Queuing theory.
E. demonstrate the ability to solve mathematical problem with fuzzy logic.

Syllabus

UNIT – I

Linear Algebra:

Vector Space , Subspace, Basis & dimensions, Change of Basis, Linear Transformation, Matrix Representation of Linear Transformation.

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MTMAN 101	BS	Advanced Mathematics	60	20	20	-	-	3	0	0	3

UNIT – II

Numerical Solution of Partial Differential Equations:

Classification of second order equations, Finite difference approximation to derivatives, Elliptic equations, Solution of Laplace's equation, Solution of Poisson's equations, Parabolic equations, Solutions of Heat equations, Hyperbolic equations.

UNIT – III

Probability & Statistics:

Probability, Compound probability, Discrete Random Variable, Binomial and Poisson distribution, Continuous random variable, Normal distribution, Sampling distribution, Theory of hypothesis.

UNIT – IV

Stochastic Process & Queuing Theory:

Introduction of random or stochastic processes, Markov processes, Markov chain, Queuing theory: M/M/1: ∞/∞/FCFS, M/M/1: N/∞/FCFS.

UNIT – V

Fuzzy Set and Theorems:

Fuzzy sets, Fuzzy relation, Fuzzy arithmetic, Fuzzy logic.

Texts:

1. Higher Engg. Mathematics: B. S. Grewal, Khanna Publishers, Delhi
2. Higher Engg. Mathematics: E. Kreyzig, John Wiley & Sons (Asia) Pvt. Ltd.
3. Operation Research: S. D. Sharma, Kedar Nath and Ram Nath, Delhi.
4. Probability, Random variables & Random processes: Schaum's outlines.
5. Stochastic processes: J. Medhi, New age international publishers.
6. Calculus of finite differences and Numerica Analysis: Gupta and Malik.
7. Fuzzy logic in Engineering: T. J. Ross.
8. Fuzzy set theory and its applications: H. J. Zimmersoms.

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M.Tech. in VLSI Design w.e.f. 2025

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MTVD101		FPGA Based System Design	60	20	20	30	20	3	0	2	4

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; C - Credit.
***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Educational Objectives (CEOs):

1. To understand the fundamentals of FPGA architecture, Verilog HDL constructs, and the complete FPGA design flow.
2. To develop skills to design, simulate, and implement combinational, sequential, and system-level digital circuits on FPGA using Verilog.
3. To apply FPGA-based system design concepts to solve real-world problems through mini-projects and case studies.

Course Outcomes (COs):

After the successful completion of this course, the student will be able to:

1. Write Verilog HDL codes using different modeling styles and verify functionality through simulation and FPGA implementation.
2. Design and realize combinational, sequential, and FSM-based digital systems on FPGA boards.
3. Integrate peripheral interfaces and apply FPGA-based solutions to practical applications using Verilog.

Syllabus:

UNIT I **8 Hrs.**

Introduction to FPGA Architecture and Design Flow

Overview of FPGA Technology: Evolution from PLDs to FPGAs, FPGA vs CPLD vs ASIC, FPGA Architecture: Configurable Logic Blocks (CLBs), Look-Up Tables (LUTs), Flip-Flops, Multiplexers, Interconnects and Routing, Input/Output Blocks, On-chip memory & DSP blocks. FPGA Vendors & Devices: Xilinx, Intel (Altera), Lattice, Microsemi.
FPGA Design Flow: Design entry, synthesis, simulation, implementation, bitstream generation. Overview of toolchains: Vivado, Quartus, Cadence

UNIT II **7 Hrs.**

Combinational Logic Design using Verilog

Verilog/ System Verilog fundamentals, Behavioral, structural, and dataflow modelling. Design Hierarchy and Modular Coding. Testbenches & Simulation: Functional vs timing simulation. Use of ModelSim/Xcelium Simulator.

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Design examples: Encoders, decoders, comparators, Multiplexers, demultiplexers, Arithmetic circuits: adders, subtractors, ALU design, Parameterization and generate statements.

UNIT III **6 Hrs.**

Sequential Logic Design using Verilog

Sequential elements: Latches, flip-flops, registers, Counters and shift registers, Finite State Machines (FSMs): Moore and Mealy machine modeling in Verilog, State encoding techniques. Clocking & Timing considerations in FPGA.

UNIT IV **7 Hrs.**

Advanced Verilog Constructs and FPGA Integration

Tasks and Functions in Verilog, Testbenches and Simulation, Functional vs timing simulation. Memory modeling: ROM, RAM, FIFO using Verilog. Interfacing peripherals with FPGA: UART, switches, LEDs, 7-seg displays.

UNIT V **7 Hrs.**

System-Level Design and Applications

Design optimization: Resource sharing, pipelining, parallelism, Timing and area trade-offs, Static Timing Analysis: Setup, hold, and clock-to-Q timing, Timing analysis, case studies – PS2 Controller, VGA Controller.

Text Books:

1. S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with Verilog Design*, 3rd ed. New York, NY, USA: McGraw-Hill Higher Education, 2016.

Reference Books:

1. M. M. R. Mano and M. D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL, VHDL, and System Verilog*, 6th ed. London, U.K.: Pearson Education, 2021.
2. C. Maxfield, *Programming FPGAs: Getting Started with Verilog*, 1st ed. New York, NY, USA: McGraw-Hill Education, 2016.
3. S. Kilts, *Advanced FPGA Design: Architecture, Implementation, and Optimization*, 1st ed. New York, NY, USA: Wiley, 2007.

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MTVD101		**FPGA Based System Design**	60	20	20	30	20	3	0	2	4

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List of Experiments:

1. Introduction to FPGA Toolchain.
2. Implement AND, OR, NOT, XOR gates.
3. Design and implement encoders, decoders, multiplexers, demultiplexers using Verilog.
4. Design and simulate adders (half, full, ripple-carry, CLA), subtractor, comparator.
5. Implement D, JK flip-flops, shift registers (SISO, SIPO, PISO, PIPO) in Verilog.
6. Design and implement 4-bit up-counter, down-counter, modulo-N counter on FPGA.
7. Implement traffic light controller using Moore/Mealy FSM in Verilog.
8. Display decimal numbers (0–9) using Verilog with a 7-segment display.
9. Implement ROM and RAM models in Verilog.
10. Design a simple UART transmitter and receiver in Verilog.

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MTVD102		CMOS VLSI DESIGN	60	20	20	30	20	3	0	2	4

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Course Educational Objectives (CEOs):

1. To understand the working principles of MOS devices, second-order effects, inverter characteristics, and their impact on VLSI circuit performance.
2. To develop the ability to design, simulate, and layout CMOS-based circuits using EDA tools, including physical design and layout optimization techniques.

Course Outcomes (COs):

After the successful completion of this course, the student will be able to:

1. Analyze MOSFET behavior considering first- and second-order effects and evaluate their implications on circuit performance.
2. Design and compare CMOS logic circuits using static and dynamic styles with a focus on delay and power optimization.
3. Create optimized physical layouts of CMOS circuits using layout design rules, Euler paths, and stick diagrams.
4. Use EDA tools to simulate and verify digital CMOS circuits at schematic and layout levels.

Syllabus:

UNIT I **9 Hrs.**

VLSI design: Flow and levels of abstraction, EDA tool overview: schematic entry, simulation, layout, extraction, Design Hierarchy, Regularity, Modularity and Locality, MOSFET Construction, operation and I–V characteristics, MOSFET behavior under DC and transient conditions, Second-order effects: Body effect, Subthreshold conduction, Velocity saturation, Hot-carrier injection, Channel length modulation, Drain-induced barrier lowering (DIBL), Punch through.

UNIT II **8 Hrs.**

CMOS Inverter: DC transfer characteristics, noise margins, Beta Ratio, Switching characteristics: delay, rise/fall times, MOS Capacitances and Their Impact, Transistor sizing for performance, MOSFET models: Level 1, Level 2, and BSIM (Level 3) models: overview and applicability.

UNIT III **8 Hrs.**

Modeling: Delay modeling using RC and Elmore delay, Logical effort and path delay analysis, Power dissipation: static, dynamic, short-circuit, leakage, Power-delay trade-offs, Low power design principles and transistor-level optimization, Scaling and its types.

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MTVD102		CMOS VLSI DESIGN	60	20	20	30	20	3	0	2	4

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; C - Credit.
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UNIT IV **8 Hrs.**

Static CMOS logic: complementary and compound gates, Dynamic logic: Domino and NORA, Pass-transistor logic and transmission gates, Sequential logic: latch and flip-flop, Timing parameters: setup, hold, propagation delay, Clocking issues: skew, clock distribution, pipelining, Memory design: ROM, SRAM (6T, 8T), DRAM, Bitline and Wordline considerations, overview of sense amplifiers

UNIT V **7 Hrs.**

Stick diagrams and CMOS layout basics: Euler paths for optimal transistor ordering in logic gates, Design rules: lambda-based and micron-based, Floor planning, placement, and routing basics, Design Rule Check (DRC), LVS, and parasitic extraction, post-layout timing simulation and parasitic analysis, Advanced topics: FinFETs, SOI CMOS.

Textbooks:

1. N. H. E. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed. Boston, MA: Pearson Education, 2010.
2. S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 4th ed. New York, NY: McGraw-Hill Education, 2014.

Reference Books:

1. J. M. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits: A Design Perspective*, 2nd ed. Upper Saddle River, NJ: Pearson Education, 2003.
2. D. A. Hodges, H. G. Jackson, and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits*, 3rd ed. New York, NY: McGraw-Hill, 2003.
3. R. J. Baker, *CMOS: Circuit Design, Layout, and Simulation*, 3rd ed. Hoboken, NJ: Wiley-IEEE Press, 2010.
4. B. Razavi, *Design of Analog CMOS Integrated Circuits*, 1st ed. New York, NY: McGraw-Hill Education, 2000.
5. K. Eshraghian, D. A. Pucknell, and S. Eshraghian, *Essentials of VLSI Circuits and Systems*, 1st ed. New Delhi, India: PHI Learning Pvt. Ltd., 2005.

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COURSE CODE	CATE-GORY	COURSE NAME	TEACHING &EVALUATION SCHEME								
			THEORY			PRACTICAL		L	T	P	CREDITS
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*				
MTVD102		**CMOS VLSI DESIGN**	60	20	20	30	20	3	0	2	4

Legends: L - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; C - Credit.
***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

List of Experiments:

1. Introduction to schematic entry and simulation.
2. CMOS inverter: schematic, transient/DC analysis.
3. NAND/NOR layout using Euler path optimization.
4. D Flip-Flop design and layout.
5. Static and dynamic logic gate design.
6. SRAM cell layout and performance testing.
7. Post-layout extraction and simulation.

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MTVD123		Microelectronics: Devices to Circuits	60	20	20	-	-	3	0	0	3

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; **C** - Credit;
***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Educational Objectives (CEOs):

This course aims to:

1. Understand the fundamentals of MOS, CMOS, and BiCMOS devices and amplifiers.
2. Learn feedback, stability, and frequency response in analog circuits.
3. Gain skills in Op-Amp circuit and filter design.
4. Develop knowledge of digital logic, sequential circuits, and memory design.

Course Outcomes (COs):

After successfully completing the course students will be able to:

1. Analyse and design MOS, CMOS, Bi-CMOS, and JFET-based amplifiers, including their small and large signal behavior.
2. Understand and apply feedback, stability, and frequency response concepts in amplifier and Op-Amp circuits.
3. Design and implement operational amplifier-based circuits and various analog filters.
4. Develop combinational and sequential digital circuits, including memory design and clock strategies.

Syllabus

Unit-I: MOS Transistor **8 Hrs.**

MOS Transistor Basic,Parasitic & SPICE Model, CMOS Inverter Basics, Power Analysis, Biasing of MOS Amplifier and its behavior as an analog switch, CMOSAmplifier Configuration (CS/CG/SF), Internal cap models and high frequency modelling, JFET, structure and operation.

Unit-II: Amplifier **9 Hrs.**

Multistage and Differential Amplifier, Small Signal Operation and Differential Amplifier, MOS Differential Amplifier, Bi-CMOS Amplifier with Active Load, Multistage Amplifier, S-domain analysis, Transfer function, Poles and Zeros, High Frequency Response of CS and

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MTVD123		Microelectronics: Devices to Circuits	60	20	20	-	-	3	0	0	3

Legends: **L** - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** – Practical; **C** - Credit;
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CE Amplifier, Frequency Response of CC and SF Configuration,Frequency Response of the Differential Amplifier, Cascode Connection and its Operation.

Unit-III: Feedback Structures **7 Hrs.**

General Feedback structure and properties of negative feedback, Basic Feedback Topologies, Design of Feedback Amplifier for all configuration, Stability and Amplifier poles, Bode Plots and Frequency Compensation

Unit-IV: Filters **8 Hrs.**

Ideal Operational Amplifier and its terminals, Inverting and Non- Inverting Configuration, Integrator and Differentiator, Large Signal Operation of Op-Amp and Second order offsets, Butterworth and Chebyshev Filters,First and Second Order Filter Functions, Switched Capacitor based filters, Single-Amplifier Biquadratic Filters, Second Order LCR Resonator.

Unit-V: CMOS Logic Design **7 Hrs.**

Combinational Logic Design, Sequential Logic Design, Clock Strategies for Sequential Design, Concept of Memory & its Designing

Textbooks:

1. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill.
2. Sedra & Smith, Microelectronic Circuits, Oxford University Press.
3. M. Morris Mano, Digital Design, Pearson.

References:

1. R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, Wiley.
2. P. R. Gray, P. J. Hurst, S. Lewis, R. Meyer, Analysis and Design of Analog Integrated Circuits, Wiley.
3. Donald A. Neamen, Microelectronics: Circuit Analysis and Design, McGraw-Hill.

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MTVD133		RF IC Design	60	20	20	0	0	3	0	0	3

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Course Educational Objectives (CEOs):

1. The objective of this course is to present the concept of design and analysis of modern RF and wireless communication integrated circuits.

Course Outcomes (COs):

After the successful completion of this course, the student will be able to:

1. Apply transmission line theory and S-parameters at high frequency.
2. Identify the specifications of RF systems.
3. Classify and differentiate the trans-receiver architectures.
4. Use Apply RF concepts to design LNA and Mixer.

Syllabus:

UNIT-I **9 Hrs.**

Review of RF Theory: RF range, skin effect, behaviour of various passive components like R, L, C, at high RF, their equivalent circuits at high RF. Transmission line theory, reflection coefficient, Smith chart calculation, impedance matching, S-parameter.

UNIT-II **8 Hrs.**

Basic concepts in RF design: wireless communication standards, nonlinearity, harmonics, gain compression, desensitization, cross modulation, inter modulation distortion (IMD), input intercept point (IIP3 & IIP2), inter symbol interference, Noise, types of noise, noise analysis of active devices.

UNIT-III **8 Hrs.**

Trans-receiver Architecture: TRF receivers, heterodyne receivers, Homodyne receivers, their comparison, type RF receiver architecture and its design.

UNIT-IV **8 Hrs.**

Design concepts-1: Low noise amplifiers, Noise Reduction techniques, various topologies, comparison and design, Mixers, Linearity improvement techniques, various topologies, comparison and design, Filters- type and design.

UNIT-V **8 Hrs.**

Design Concepts-2: VCO, PLL, various types, comparison and design. Frequency synthesizes and their design IC application and case studies for DECT, GSM and Bluetooth. Layout issues in RF IC design,

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MTVD133		RF IC Design	60	20	20	0	0	3	0	0	3

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***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

TEXT BOOKS:

1. BehzadRazavi, RF Microelectronics, Third edition, Prentice Hall,2011
2. Thomas H. Lee, "The design of CMOS radio frequency integrated circuits", Second Edition, Cambridge University Press, 2012.
3. R. Ludwig and P. Bretcheko, "RF Circuit Design", Second Edition, Pearson, 2009.

REFERENCE BOOKS:

1. L. E. Larson, "RF and Microwave circuit design for wireless communication", Artech House Publication 1997.
2. Robert H. Caverly, "CMOS RFIC Design Principles", Artech House Publications, 2007.

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MTVD104		Design Verification Lab	0	0	0	30	20	0	0	4	2

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***Teacher Assessment** shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Educational Objectives (CEOs):

1. To provide hands-on experience in design and verification of digital circuits using System-Verilog.
2. To develop skills in tes tbench creation, assertions, and coverage-driven verification for both combinational and sequential circuits.
3. To prepare students for industry-oriented verification methodologies, enabling them to analyze, debug, and validate digital designs effectively.

Course Outcomes (COs):

After the successful completion of this course, the student will be able to:

1. Design and verify basic to advanced combinational and sequential circuits using System
2. Verilog.
3. Develop and apply self-checking test benches, assertions, and functional coverage to ensure robust verification.
4. Analyze and evaluate simulation results to validate circuit correctness and gain practical exposure to verification practices used in industry.

List of Experiments:

1. **Basic Logic Gates Verification**
   - Verify the functionality of AND, OR, NOT, NAND, NOR, XOR, and XNOR gates.
   - Use truth tables and directed test vectors.
2. **Half Adder & Full Adder**
   - Design and verify half adder and full adder.
   - Apply exhaustive stimulus (all input combinations).
3. **4-to-1 Multiplexer & 1-to-4 Demultiplexer**
   - Verify correct selection behavior.
   - Use randomized inputs and functional coverage.
4. **Encoder & Decoder Verification**
   - 3-to-8 decoder and 8-to-3 priority encoder.
   - Verify valid/invalid input scenarios.

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MTVD104		Design Verification Lab	0	0	0	30	20	0	0	4	2

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5. **4-bit Comparator**
   - Verify less-than, equal-to, and greater-than outputs.
   - Apply constrained-random test inputs.
6. **4-bit Arithmetic Circuits (Adder-Subtractor)**
   - Verify an ALU slice that performs add/subtract operations.
   - Include corner cases like overflow and underflow.
7. **4-bit Parity Generator & Checker**
   - Verify even and odd parity generation.
   - Check detection of single-bit errors.
8. **4-bit Magnitude Comparator with Assertions**
   - Add **SystemVerilog assertions (SVA)** to validate correctness.
   - Verify using randomized tests.
9. **4-bit Synchronous Counter (Up/Down Counter)**
   - Verify counting sequence, wrap-around, and enable/reset conditions.
   - Use functional coverage to ensure all states are visited.
10. **Counter Verification with Self-Checking Testbench**
    - Develop a scoreboard-based verification for a 4-bit counter.
    - Verify normal operation, asynchronous/synchronous reset, load, and enable.
    - Collect coverage to ensure complete verification.