



Shri Vaishnav Vidyapeeth Vishwavidyalaya
Shri Vaishnav Institute of Technology and Science
Choice Based Credit System (CBCS) Scheme in the light of NEP-2020
B.Tech. in EC-VLSI

SEMESTER-V (2024-2028)

SEMESTER - V (2024-2025)												
S. No.	COURSE CODE	COURSE NAME	TEACHING SCHEME/WEEK			CREDITS	EXAMINATION SCHEME					TOTAL MARKS
			L	T	P		THEORY			PRACTICAL		
							End Sem University Exam (60%)	Two Term Exam (20%)	Teachers Assessment* (20%)	End Sem University Exam (60%)	Teachers Assessment* (40%)	
1	BTEVD503	VLSI Principles, RTL Design and Verification	3	0	2	4	60	20	20	30	20	150
2	BTEC504	CMOS VLSI Design	3	1	2	5	60	20	20	30	20	150
3	-	Elective I	3	0	2	4	60	20	20	30	20	150
4	-	Generic Elective II	4	0	0	4	60	20	20	0	0	100
5	BTEVD502	Semiconductor Materials Synthesis and Characterization	3	0	0	3	60	20	20	0	0	100
6	BTEC507	Programming in Python	0	0	2	1	0	0	0	30	20	50
7	BTEEE501	Minor Project	0	0	4	2	0	0	0	30	20	50
8	BTEEE502	PLC Lab	0	0	4	2	0	0	0	30	20	50
TOTAL			16	1	16	25	300	100	100	180	120	800

Legends: L - Lecture ; T - Tutorial/Teacher Guided Student Activity ; P - Practical ;

*Teacher Assessment shall be based on following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.

S. No.	Course Code	Elective I
1	BTEC525N	FPGA Based System Design
2	BTEI611	Data Acquisition Systems
3	BTECIOT508	Introduction to AI and ML

Chairperson
Chairperson
Board of Studies
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore

Chairperson
Chairperson
Faculty of Studies
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore

Controller of Examinations
Controller of Examinations
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore

Registrar
Registrar
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore

Vice Chancellor
Vice Chancellor
Shri Vaishnav Vidyapeeth
Vishwavidyalaya, Indore