Shri Vaishnav Vidyapeeth Vishwavidyalaya
Shri Vaishnav Institute of Technology and Science
Choice Based Credit System (CBCS) Scheme in the light of NEP-2020
B.Tech. in Electrical and Electronics Engineering (Semiconductor Chip Design and VLSI - L&T Edutech)
SEMESTER-III (2025-2029)

S. No.	COURSE CODE	COURSE NAME	TEACHING SCHEME/WEEK			CREDITS	EXAMINATION SCHEME					TOTAL MARKS
							THEORY			PRACTICAL		
			L	T	P		End Sem Unversity Exam (60%)	Two Term Exam (20%)	Teachers Assess-ment* (20%)	End Sem Unversity Exam (60%)	Teachers Assess-ment* (40%)	
1	BTVDLT301	Embedded Computing Principal	2	0	2	3	60	20	20	30	20	150
2	BTEC302	Network Analysis and Synthesis	3	1	2	5	60	20	20	30	20	150
3	BTECIOT401	Sensors and Signal Conditioning	3	0	2	4	60	20	20	30	20	150
4	BTEC304	Electronic Devices and Circuits	3	0	2	4	60	20	20	30	20	150
5	-	Generic Elective I	4	0	0	4	60	20	20	0	0	100
6	BTEC308	Design Lab	0	0	2	1	0	0	0	30	20	50
TOTAL			**15**	**1**	**10**	**21**	**300**	**100**	**100**	**150**	**100**	**750**

Legends: L - Lecture ; T - Tutorial/Teacher Guided Student Activity ; P - Practical ;

***Teacher Assessment shall be based on following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.**

16/7/2026

Chairperson
Board of Studies
Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore

Chairperson
Faculty of Studies
Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore

Controller of Examinations
Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore

16/07/26

Registrar
Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore

Vice Chancellor
Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore