		Shri Vaishnav Vidy	apeet	h Vi	shwa	avidy	/alaya,	Indo	ore (M	P)			
		Choice B	ased Cre	edit Sy	stem (CBCS)	Scheme						
		M.Tech. in E					f. July 20	20)		3			
	1		<u> </u>	SEME	STER		r			2			
Sr. No.		Name of Subject	Course Code	Teaching Scheme/ Week			Examination Scheme						4 1
						-	Theory			Practical		Total	
				L	т	Р	End Sem Unversity Exam	Two Term Exam	Teachers Asses- ment*	End Sem Unversity Exam	Teachers Asses- ment*	Marks	Credits
1	MTES201	Advanced Microcontroller		2	1	2	60	20	20	- 30	20	150	4
2	MTDC202	Advanced Digital Signal Processing		2	0	2	60	20	20	30	20	150	3
3	MTES202	Real Time Operating Systems		3	0	2	60	20	20	30	20	150	4
4	MTES213/	Elective: 1 Machine Learning 2 Artificial Intelligence 3 Hardware/Software Codesign		3	0	0	60	20	20	0	0	100	3
5		Elective: 1 Sensors and Actuators 2 Internet of Things 3 Wireless Sensor Networks		3	0	2	60	20	20	30	20	150	4
TOTAL					1	8	300	100	100	120	80	700	18
*Tea mor	acher Assessm e than 10 mark	ent shall be based on following components s.	: Quiz/As	signme	ent/Pro	ject/Pa	rticipation i	n Clas	s, given th	nat no com	ponent sh	nall exc	eed

Students are advised to take online MOOCS course of minimum two credits

Neep ..

Chairperson **Board of Studies** Shri Vaishnav Vidyapeeth Vishwavidyalaya Indore

Nebto

Chairperson Faculty of Studies Shri Vaishnav Vidyapeeth Vishwavidyalaya, INDORE

Registrar Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore

an

Controller of Examinations Shri Vaishnav Vidyapeeth Vishwavidyalay

totoar

Vice Chancellor Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore