Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore Shri Vaishnav Institute of Technology and Science Choice Based Credit System (CBCS) in the Light of NEP-2020 B.Tech. in Electronics and Instrumentation

(Common to EI/MX/EE/EX/RW)

(2021-2025)

COURSE CATE		8	T	EACHIN	G &EVAL	LUATIO	N SCI	HEME			
		THEORY			PRACT	ICAL				235-	
CODE	COURSE CATE- CODE GORY COURSE NAME	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	T	P	CREDITS	
BTEI401	DCC	Microprocessor and Microcontroller	60	20	20	30	20	3	1	2	5

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit;

Input-Output interfacing: Peripherals I/O. PPI 8255 Architecture and modes of operation, Interfacing to 16-bit microprocessor and programming, DMA controller (8257) Architecture, Programmable interval timer 8254, USART 8251.

UNIT III

8 Hrs.

Introduction to 8051 Microcontroller

Introduction, Difference between Microprocessors and Microcontrollers. Overview of 8051 Microcontroller family, Architecture of 8051 Microcontroller, The program counter and ROM space in the 8051, registers, 8051 register banks.

UNIT IV

10Hrs.

8051 Assembly Language Programming

Introduction to 8051 assembly programming, Structure of Assembly language, Assembling and running an 8051 program, 8051 data types and directives, interrupts

8051 Addressing Modes & Instruction set

Addressing modes, Accessing memory using various Addressing modes, Bit addresses for I/O and RAM, Arithmetic instructions, Signed number concepts and arithmetic operations, Logic and compare instructions, Rotate instruction, Jump, Loop, And Call Instructions, Call instructions time delay for various 8051 chips.

UNIT V

10 Hrs.

8051 Programming in C

Data types and time delay in 8051 C, I/O programming in 8051 C, Logic operations in 8051 C, Data conversion programs in 8051 C, Accessing code ROM space in 8051 C, Interfacing with LEDs, LCDs ADCs, DACs.

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Faculty of Studies Shri Vaishnav Vidyapeeth Vishwasidyalaya, Indore Controller of Examinations

Shri Valshnav Vidyapeeth Vishwavidyalaya, Indore

^{*}Teacher Assessment shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore Shri Vaishnav Institute of Technology and Science

Choice Based Credit System (CBCS) in the Light of NEP-2020 B.Tech. in Electronics and Instrumentation

(Common to EI/MX/EE/EX/RW)

(2021-2025)

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CODE	CAUDELY	COURSE NAME	END SEN University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	т	T P	CREDITS	
BTEI401	DCC	Microprocessor and Microcontroller	60	20	20	30	20	3	1	2	5	

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit;

Text Books:

- 1. A.K. Ray & K.M. Bhurchandi, "Advanced Microprocessors and peripheral-Architecture, Programming and Interfacing", Tata McGraw –Hill, 2012.
- Muhammad Ali Mazidi, Janice Gillispie Mazidi and Rolin McKinlay, "The 8051
 Microcontroller and Embedded Systems Using Assembly and C, 2/e", Second Edition, Pearson
 Education 2008.
- Kenneth J. Ayala, Dhananjay V. Gadre, "The 8051 Microcontroller & Embedded Systems using Assembly and C", Cengage Learning, India Edition, 2008.

References:

- Douglas V. Hall , "Microprocessor and interfacing", Revised second edition, Macmillan, McGraw Hill 2006.
- Han Way Huang, "Using the MCS-51 Microcontrollers", Oxford Uni Press, 2000.
- Rajkamal ,"Microcontrollers Architecture, programming, interfacing and system design" Pearson education. 2009.

List of Experiments:

- Introduction to 8086 & 8051 kit, hardware features & modes of operationand Technique of programming & basic commands of kit.
- Design programs for Arithmetic Operations.
- 3. Develop a program to find 1's complement and then 2's complement of a 16-bit numbers.
- Develop a program to find larger of two numbers.
- 5. Write a program to shift an 8-bit number left by 2-bits.
- 6. Write a program to generate a square wave of 2 KHz Frequency on input pin.
- 7. Introduction to IDE and Assembler directives.
- Develop 8051 Assembly language programs using Arithmetic/ Logical instructions.
- 8051 Assembly language programming for block data transfer between internal and external memory including overlapping blocks.

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Shri Valshoav Vidyapeeth Vishwavidyalaya, Indore Joint Registrar

Vishwavidyalaya, Indore

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Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore Shri Vaishnav Institute of Technology and Science

Choice Based Credit System (CBCS) in the Light of NEP-2020 B.Tech. in Electronics and Instrumentation

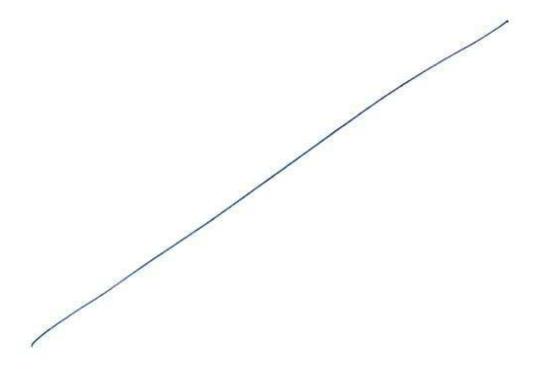
(Common to EI/MX/EE/EX/RW)

(2021-2025)

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	COURSE NAME	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	т	Р	CREDITS	
BTEI401	DCC	Microprocessor and Microcontroller	60	20	20	30	20	3	1	2	5

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit;

- 10. 8051 Assembly language programming for
 - a. code conversions
 - b. Timers in different modes.
 - c. I/O port programming in embedded C.
 - d. Programming of LCD in embedded C.



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Name of Program: Bachelor of Technology in Electronics & Communication

	SUBJECT Cate-			TE.	ACHINO	G &EVA	LUATIO	N SC	CHE	ME	
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CODE	Cate- gory	SUBJECT NAME	END SEM University Exam	Two Term Exam	Teachers Assess- ment*	END SEM University Exam	Teachers Assess- ment*	L	Т	P	CREDITS
BTEC502	EC	Cellular and Mobile Communication	60	20	20	0	0	3	0	0	3

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit;

Course Educational Objectives (CEOs):

The subject aims to provide the student with:

- To impart fundamental concepts in cellular technology, models of mobile radio channels, communication technologies adapted and wireless networks.
- 2. Be acquainted with different interference factors influencing cellular and mobile communications.
- 3. To efficiently use the background behind developing different path loss and/or radio coverage in cellular environment.
- 4. To expose the students to the most recent technological developments in mobile communication systems.

Course Outcomes (COs):

- 1. Students will get familiar with cellular terminology as mobile station, base station and mobile telephone switching office.
- 2. Develop the capability to analyze and design propagation models for mobile radio channel.
- 3. Learn how to reduce co-channel and non co-channel interference.
- 4. Know about implementation of digital cellular system.

Syllabus

UNIT I 8 Hrs.

Introduction to Cellular Mobile Systems: Limitations of Conventional Mobile Telephone System, Basic Cellular Systems, Performance Criteria, Free-Space propagation model for mobile communication, Radio Propagation mechanism: reflection, diffraction, scattering and interference.

UNIT II 9 Hrs.

Cellular Concept: Operations of Cellular system, Concept of Frequency Reuse, Co-channel Interference Reduction Factor, Desired C/I in an Omni-directional Antenna System, Sectoring and Cell Splitting, System Capacity, Trunking and Grade of Service (GOS), Concept of Handoff, Types of Handoff, Queuing of Handoff.

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UNIT III 8 Hrs.

Cell Coverage for Signal and Traffic: Signal Reflections in Flat and Hilly Terrain, Effect of Human Made Structures, Phase Difference between Direct and Reflected Paths, Straight Line Path Loss Slope, General Formula for Mobile Propagation between Two Fixed Station over Water and Flat Open Area, Near and Long Distance Propagation, Point to Point model.

UNIT IV 9 Hrs.

Interference in Cellular Mobile System: Co-channel Interference: Interference in co-channel cell, comparison N=4 and N=7 cellular system. Non Co-channel Interference: Adjacent-Channel Interference, Next Channel Interference and Neighboring Channel Interference, Near-End Far-End Interference, Rake receiver

Frequency Management, Channel Assignment: Numbering the radio channels, Set-up Channels, Channel Assignment Schemes: Fixed and Dynamic Channel Assignment Schemes, Sharing and Borrowing concept.

UNIT V 8 Hrs.

Digital Cellular System: Multiple Access Techniques – FDMA, TDMA and CDMA, GSM System Architecture, GSM Radio Subsystem, GSM Channel Types, Frame Structure for GSM, Signal Processing in GSM.

Text Books:

- William C. Y. Lee, "Mobile Cellular Telecommunications: Analog and Digital Systems", 2nd Edition, Tata McGraw Hill Publication, 2017.
- 2. Theodore S. Rappaport, "Wireless Communications: Principles and Practice", 2nd Edition, Pearson / PHI Publication, 2010.

References:

- 1. Iti Saha Misra, "Wireless Communications and Networks: 3G and Beyond, 2nd Edition", Tata McGraw Hill Publication, 2013.
- 2. Gordon L. Stuber, "Principles of Mobile Communications", Springer International 2nd Edition, 2007.
- 3. William Stallings, "Wireless Communications and Networks", 2nd Edition, Pearson Education, 2005.
- 4. Siegmund M. Redl, Mathias K. Weber, Malcolm W. Oliphant, "An Introduction to GSM", Artech House Publishers, 1998.

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Name of Program: Bachelor of Technology in Electronics & Communication

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SUBJECT Catagory		7	HEORY	7	PRAC	ΓICAL					
CODE	Category	SUBJECT NAME	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	т	P	CREDITS
BTEC504	EC	CMOS VLSI Design	60	20	20	30	20	3	1	2	5

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit;

Course Educational Objectives (CEOs):

To inculcate the concepts of CMOS VLSI Design and relate its importance in today's scenario. To impart knowledge based on design of analog as well as digital VLSI circuits.

Course Outcomes (COs):

After completion of this course the students are expected to be able to demonstrate following knowledge, skills and attitudes

The students will be able to:

- 1. Demonstrate the working and device physics related to CMOS.
- 2. Design circuits based on combinational logic.
- 3. Design analog circuits related to CMOS.
- 4. Draw stick diagrams and design layouts for different devices and circuits.

Syllabus

UNIT I

9 Hrs.

Introduction / Orientation: VLSI Design flow, Y- Chart, Structured design strategies: Hierarchy, Regularity, Modularity and Locality. Design Methods: Microprocessor/DSP, Programmable Logic, GA and SOG, Cell based design, Full custom Design; Platform based design/SOC. Design Economics.

UNIT II

10 Hrs.

MOS Transistor Theory: MOS device equations, Second order effects: Mobility degradation and velocity saturation, Body effect, Short channel effects, Narrow width effects. CMOS Inverter DC Characteristics-VI Characteristics, Beta Ratio effects, Noise Margin. Scaling - Transistor Scaling, Supply Voltage Scaling, Interconnect Scaling.

UNIT III

9 Hrs.

Delay and Power Considerations: Delay Definitions, Transient response, RC Delay model, Linear Delay Model. CMOS Logic implementations and Logical Effort. Power Definitions, Dynamic Power, Static Power, Latch up triggering and prevention.

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UNIT IV

8 Hrs.

CMOS Processing Technology: Wafer Formation, Photolithography, N-well process, Twin tub process, Stick Diagrams, layout design rules, CMOS process enhancements.

UNIT IV

9 Hrs.

Analog CMOS design: Introduction to analog design, Current Mirror, Single stage amplifier: Common source with diode, resistive and current source connected load, Source follower, Differential amplifiers. Frequency response: Miller effect, Association of Poles with nodes, common source stage and source followers.

Text Books:

- 1. Neil H.E. Weste, David Money Harris, "CMOS VLSI Design, A circuits and systems perspective", 4th Edition, Pearson, 2010.
- 2. Neil H.E. Weste, David Money Harris Ayan Banerjee, "CMOS VLSI Design, A circuits and systems perspective", 4th Edition, Pearson Education, 2010.
- 3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill Education, 2016.
- 4. Peter Van Zant, "Microchip Fabrication, A Practical Guide to Semiconductor Processing", 6th Edition, McGraw Hill Professional, 2013.

References:

- 1. Sung Mo Kang, Yusuf Lebliabici, "CMOS Digital Integrated Circuits: Analysis and Design", 4th Edition, Tata McGraw Hill, 2015.
- 2. Douglas A. Pucknell, Kamran Eshraghian, "Basic VLSI Design",3rd Edition, Prentice Hall, 1994.
- 3. S. M. Sze, VLSI Technology, 2nd Edition, Tata McGraw-Hill Education, 2003.

List of Experiments:

- 1. Introduction to layout EDA tools and Technologies.
- 2. Study of Stick Diagrams and Euler's Path.
- 3. Layout Design of Resistors, Capacitors and MOSFETS.
- 4. Layout Design for Logic gates.
- 5. Layout Design for Half adder and Full adder.
- 6. Layout Design for Multiplexer.
- 7. Layout Design for Encoders and Decoders.
- 8. Layout Design for SRAM.
- 9. Layout Design for Flip Flops.
- 10. Layout Design for 4-Bit Multiplier.
- 11. Study of different packages and Bonding pads.

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Name of Program: Bachelor of Technology in Electronics & Communication

	-			TE	ACHING	& EVAL	UATION	SCHE	ME		
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SUBJECT CODE	CATEGORY	SUBJECT NAME	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	т	P	CREDITS
BTEC525	EC	FPGA Based System Design	60	20	20	30	20	3	1	2	5

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit;

Course Educational Objectives

The objective of this course is to-

- 1. Introduce basic concepts of Verilog Hardware Description Language.
- 2. Describe FPGA implementation of digital systems.

Course Outcomes

After completion of this course the students will be able to-

- 1. Describe digital hardware in terms of its structure or behavior using Verilog HDL.
- 2. Configure FPGA boards for specific design need.

Syllabus

UNIT I 9 Hrs.

Programmable Logic Devices and Computer Aided Design Tools:

Introduction to design of digital hardware, Programmable Logic Devices- PAL, PLA, CPLD and FPGA.CAD Tools: Introduction, Design flow, Synthesis, RTL Synthesis, Overview of Synthesis Steps, Net List Generation, Gate Optimization, Technology Mapping, Simulation, Functional and Timing Simulation, Physical Design Steps- Placement, Routing and Static Timing Analysis.

UNIT II 9 Hrs.

Verilog HDL Basics

Introduction of HDL, Verilog and VHDL, Top Down and Bottom Up design, Data Flow Modeling, Structure and Behavioral Modeling, Verilog Basic Constructs, White Space, Comments, Nets and Variables, Data Types, Identifiers, Signal Values, Numbers, Parameters.

Module and Ports- Module Declaration, List of Ports, Port Types, Port Declaration, Port Connection Rules.

UNIT III 9 Hrs.

Concurrent Statements

Verilog Operators: Arithmetic, Bitwise, Logical, Reduction, Relational, Shift, Conditional, Concatenation, Replication. Operator Precedence, Gate Instantiation, Signal Assignments, Continuous Assignment, Delays, Data Flow Modeling and Structure Modeling, Module Instantiation, Design of various Combinational Logic Circuits i.e. Adders, Multiplexers, Encoders and Decoders.

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Shri Vaishnav Vidyapeeth Vishwavidyalaya

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UNIT IV 9 Hrs.

Procedural Statements

Always and Initial Block, Sensitivity List, Blocking and Non Blocking Assignments, If-else Statements, Case Statements, For Loop, While Loop, Repeat and Forever Loop, Generate statement, Verilog Function and Task, Finite State Machines- Melay and Moore Models, Behavioral Modeling of Various Combinational Circuits. Behavioral Modeling of Various Sequential Circuits- Latches and Flip Flops, Shift Registers and Counters, Mealy and Moore Finite State Machines.

UNIT V 9 Hrs.

Test Bench

Verification Concepts, Test Bench Overview, Linear Test bench, File I/O Based Test bench, State Machine based Test bench, Task based Test bench, Self Checking Test bench, Stimulus Generator, Bus Functional Models, Driver, Receiver, Protocol Monitor, Scoreboard, Checker, Coverage. Code Coverage, Functional Coverage, Task and Function.

Text Books:

- Stephen Brown I Zvanko Vranesic, "Fundamentals of Digital Logic with Verilog Design", 3rd Edition, Mc Graw Hill, 2014.
- 2. Samir Palnitkar: Verilog HDL A Guide to Digital Design and Synthesis, 2nd Edition, Pearson, , 2003.

References:

- 1. Peter Wilson: Design Recipes for FPGA using Verilog and VHDL, 2nd Edition, Newnes Publication, 2016.
- 2. M. Morris Mano, Michael D. Cilletti: Digital Design With An Introduction to The Verilog HDL, 5th Edition, Pearson, 2012.

List of Experiments:

Students should implement and verify digital logic design using Verilog HDL. After synthesis and simulation the design should be implemented on FPGA board.

- 1. Design of Boolean Functions using Gate Instantiation.
- 2. Design of various Adders Circuits.
- 3. Design of various Multiplexers.
- 4. Design and analysis of Encoder and Decoders.
- 5. Design of various Latches and Flip Flops with Preset and Clear capability.
- 6. Design of various Shift registers.
- 7. Design Johnson and Ring counters.
- 8. Design Synchronous and Asynchronous Up/Down Counters.
- 9. Design of Frequency Divider Circuit.
- 10. Design of Mealy and Moore Finite State Machines.

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Name of Program: Bachelor of Technology in Electronics & Communication

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SUBJECT CODE	Categ	SUBJECT NAME	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	Т	P	CREDITS
BTEI611	EC	Data Acquisition System	60	20	20	30	20	3	1	2	5

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit;

Course Educational Objectives (CEOs):

- 1. To know about the types of transducers and display systems associated with it.
- 2. To understand the function of Data Acquisition system.
- 3. To gain information about data acquisition, data logging and application of sensors in condition based monitoring.
- 4. To learn about communication devices used in Data Acquisition system.

Course Outcomes (COs):

The students will be able to

- 1. Summarize the working and construction of sensors measuring various physical parameters.
- 2. Outline operations of various data acquisition and transmission systems.
- 3. Distinguish smart sensors from normal sensors by their operation and construction.
- 4. Classify various sensing methods used in condition monitoring.

Syllabus:

UNIT-I 7hr.

Introduction to Display System: Seven segment, Dot matrix, Multiplexed, Code converter, LCD(construction ,principle), Plasma and vapor displays. Nixie Tube and its principle, OLED, Discharge tubes, application of display systems, interfacing with LED, interfacing with LCD.

UNIT- II 10hr.

Recorders: Galvanometric type, Null type, Potentiometer type, Strip Chart and circular charttype, Magnetic tape recorder, principle & operation, Digital tape recorders, Optical storage disk, recorders applications in data acquisition system. Computer control introduction: Need of computer in a control system-Functional block diagram of a computer control system-Data loggers- Supervisory computer control.

UNIT-III

12hr.

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General Telemetric Systems: land line & RF telemetry, voltage, current and Position telemetry with feedback mechanism, RF telemetry, Amplitude modulation, Frequency modulation, Pulse modulation, pulse amplitude modulation, pulse code modulation, Microwave channels, Radio ink, Transmitting and receiving antenna, telemetry with time and frequency division multiplexing, telemetry hardware.

UNIT-IV 12hr.

Data Acquisition System(DAS): single channel and multi channel, SuperVisory control and data acquisition system(SCADA), data acquisition system around microprocessor, micro controller & PC, Introduction to PLC: Evolution of PLC's – Sequential and programmable controllers – Architecture-Programming of PLC – Relay

logic - Ladder logic, and its IEEE standard..

UNIT-V 10hr.

Requirement of communication networks of PLC - connecting PLC to computer - Interlocks and alarms - Case

study of Tank level control system, Data transfer techniques: DMA controller and data transfer in DMA mode, Serial data transmission methods, RS - 232C: specifications connection and timing, RS-422,RS-423 applications GPIB/IEEE-488 standard digital interface use, parallel communication applications in DAS, Local Area networks and its standard, Universal serial bus design with its application, Foundation –Fieldbus, ModBus, TCP/IP.

Text Books:

- 1. Murty D V S, "Transducers & Instrumentation", PHI, New Delhi (2016)
- 2. Sawhney A K, "Electrical and Electronics Measurements and Instrumentation", Dhanpat Rai and Sons.(2015)

References:

- 1. Mathivanan N "Microprocessor PC Hardware and interfacing", PHI, New delhi
- 2. H S Kalsi "Electronic Instrumentation" TMH, New delhi (2012)
- 3. Patranabis-Principles of Industrial Instrumentation 3rd Ed., TMH(2009)
- 4. D.Roy Choudhury and Shail B.Jain, Linear Integrated circuits, New age International Pvt. Ltd, 2003.

List of Experiments:

- 1. To learn about basics of LabView and its HMI(Human Machine Interface).
- 2. To Study the Various Palettes Used in LabView to create virtual instruments.
- 3. To perform and Study of Creation of Virtual Instruments, (Creation of Random Wave Analyzer.)
- 4. Implement Virtual Instrument (Random Wave Analyzer) & Control its Wave plot Speed by adding Time Delay.
- 5. Develop Virtual Instrument (Random Plot Analyzer) and Also add a function that will calculate the mean values of Plot.
- 6. Design a HMI of PLC using LabView.
- 7. Develop HMI using LabView for Fahrenheit (°F) to Celsius (°C).

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- 8. Design a table to create data logging.
- 9. Write a program for table of 2 using loop.
- 10. Design a HMI to display sine wave

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ShriVaishnavVidyapeethVishwavidyalaya B.Tech/B.Tech+MBA(CSE) and B.Tech+M.Tech(CSE/CSE-CC/CSE-CF/CSE-BDA) Choice Based Credit System (CBCS)-2018-19

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COURSE CODE	CATEGORY	COURSE NAME	L	Т	P	CREDITS	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	
BTCS403		Data	3	1	2	5	60	20	20	30	20
D1 C5403	UG	Structure and		_	_		00	20	20		20
		Algorithms									

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit; *Teacher Assessment shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Objectives:

- 1. To understand efficient storage mechanisms of data for an easy access.
- 2. To design and implementation of various basic and advanced data structures.
- 3. To introduce various techniques for representation of the data in the real world.
- 4. To develop application using data structures.
- 5. To understand the concept of protection and management of data.

Course Outcomes:

Upon the completion of the course, students will be able to:

- 1. Get a good understanding of applications of Data Structures.
- 2. Develop application using data structures.
- 3. Handle operations like searching, insertion, deletion, traversing mechanism etc.on various data structures.
- 4. Decide the appropriate data type and data structure for a given problem.
- 5. Select the best algorithm to solve a problem by considering various problem characteristics, such as the data size, the type of operations, etc.

Syllabus:

UNIT I

Introduction: Overview of Data structures, Types of data structures, Primitive and Non Primitive data structures and Operations, Introduction to Algorithms & complexity notations. Characteristic of Array, One Dimensional Array, Operation with Array, Two Dimensional Arrays, Three or Multi-Dimensional Arrays, Sparse matrix, Drawbacks of linear arrays. Strings, Array of Structures, Pointer and one dimensional Arrays, Pointers and Two Dimensional Arrays, Pointers and Structure.

UNIT II

Linked List: Linked List as an ADT, Linked List Vs. Arrays, Dynamic Memory Allocation & De-allocation for a Linked List, Types of Linked List: Circular & Doubly Linked List. Linked List operations: All possible insertions and deletion operations on all types of Linked list Reverse a Single Linked List; Divide a singly linked list into two equal halves, Application of Linked List.

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Joint Registrar

ShriVaishnavVidyapeethVishwavidyalaya B.Tech/B.Tech+MBA(CSE) and B.Tech+M.Tech(CSE/CSE-CC/CSE-CF/CSE-BDA) Choice Based Credit System (CBCS)-2018-19

UNIT III

Stack: The Stack as an ADT, Stack operation, Array Representation of Stack, Link Representation of Stack, Application of stack – Recursion, Polish Notation . Types of Recursion, problem based on Recursion: Tower of Hanoi

The Queue: The Queue as an ADT, Queue operation, Array Representation of Queue, Linked Representation of Queue, Types of Queue: Circular Queue & Dequeue, Introduction of Priority Queue, Application of Queues.

UNIT IV

Tree: Definitions and Concepts of Binary trees, Types of Binary Tree, Representation of Binary tree: Array & Linked List. General tree, forest, Expression Tree. Forest and general tree to binary tree conversion. Binary Search Tree Creation, Operations on Binary Search Trees: insertion, deletion & Search an element, Traversals on Binary SEARCH TREE and algorithms. Height balanced Tree: AVL, B-Tree, 2-3 Tree, B+Tree: Creation, Insertion & Deletion.

Graph: Definitions and Concepts Graph Representations: Adjacency MATRIX, Incidence matrix, Graph TRAVERSAL (DFS & BFS), Spanning Tree and Minimum Cost Spanning Tree: Prim's & Kruskal's Algorithm.

UNIT V

Sortings: Sorting Concept and types of Sorting, Stable & Unstable sorting. Concept of Insertion Sort, Selection sort, Bubble sort, Quick Sort, Merge Sort, Heap & Heap Sort, Shell Sort & Radix sort. Algorithms and performance of Insertion, selection, bubble, Quick sort & Merge sort.

Text Books:

- 1. Ashok N. Kamthane, "Introduction to Data structures", 2nd Edition, Pearson Education India,2011.
- 2. Tremblay & Sorenson, "Introduction to Data- Structure with applications", 8th Edition, Tata McGrawHill,2011.
- 3. Bhagat Singh & Thomas Naps, "Introduction to Data structure", 2nd Edition, Tata McGrawHill 2009.
- 4. Robert Kruse, "Data Structures and Program Design", 2nd Edition, PHI, 1997.
- 5. Lipschutz Seymour,"Data structures with C",1st Edition,Mc-GrawHill,2017.

References:

- 1. Rajesh K. Shukla ,Data Structures Using C & C++, Wiley-India 2016.
- 2. ISRD Group ,Data Structures Using C, TataMcGraw-Hill 2015.
- 3. E. Balagurusamy,"Data Structure Using C", Tata McGraw-Hill 2017.
- 4. Prof. P.S. Deshpande, Prof. O.G. Kakde, C & Data Structures, Charles River Media 2015.
- 5. Gav Pai, Data Structures, Tata McGraw-Hill, 2015.

List of Practical:

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ShriVaishnavVidyapeethVishwavidyalaya B.Tech/B.Tech+MBA(CSE) and B.Tech+M.Tech(CSE/CSE-CC/CSE-CF/CSE-BDA) Choice Based Credit System (CBCS)-2018-19

- 1. To develop a program to find an average of an array using AVG function.
- 2. To implement a program that can insert, delete and edit an element in array.
- 3. To implement an algorithm for insert and delete operations of circular queue and implement the same using array.
- 4. Write a menu driven program to implement the push, pop and display option of the stack with the help of static memory allocation.
- 5. Write a menu driven program to implement the push, pop and display option of the stack with the help of dynamic memory allocation.
- 6. Write a menu driven program to implementing the various operations on a linear queue with the help of static memory allocation.
- 7. Write a menu driven program to implementing the various operations on a linear queue with the help of dynamic memory allocation.
- 8. Write a menu driven program to implement various operations on a linear linked list.
- 9. Write a menu driven program to implement various operations on a circular linked list
- 10. Program for implementation of Bubble sort
- 11. Program for Insertion sort
- 12. Program for Merge Sort
- 13. Program to implement Heap sort
- 14. Program to implement Quick sort
- 15. Program to Construct a Binary Search Tree and perform deletion, inorder traversal on it
- 16. To develop an algorithm for binary tree operations and implement the same.
- 17. To design an algorithm for sequential search, implement and test it.
- 18. To develop an algorithm for binary search and perform the same.

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		(202	1-2025)							
				TEA	CHING	&EVALU.	ATION	SCHE	ME		
			Т	HEORY		PRACT	ICAL				
COURSE CODE	CATEG	COURSE NAME	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	Т	P	CREDITS
BTME510	AESE	DESIGN THINKING AND INNOVATION	60	20	20	0	0	2	0	0	2

 $Legends: \ L-Lecture; \ T-Tutorial/Teacher\ Guided\ Student\ Activity; \ P-Practical; \ C-Credit;$

Course Educational Objectives (CEOs):

The objective of this course is to provide (A) the new ways of creative thinking and learn the innovation cycle of design thinking process, (B) understand product design and prototyping and (C) develop innovative product.

Course Outcomes (COs):

After completion of this course student will able to

- 1. Compare and classify the various learning styles and memory techniques and apply them in their engineering education
- 2. Analyze emotional experience and inspect emotional expressions to better understand users while designing innovative products
- 3. Develop new ways of creative thinking and learn the innovation cycle of design thinking process for developing innovative products
- 4. Propose real-time innovative engineering product designs and choose appropriate frameworks, strategies, techniques during prototype development
- 5. Perceive individual differences and its impact on everyday decisions and further Create a better customer experience

Syllabus

Unit I (6 Hrs)

Learning: understanding the learning process, Kolb's learning styles, assessing and interpreting. Memory: understanding the memory process, problems in retention, memory enhancement techniques.

Emotions: understanding emotions, experience & expression, assessing empathy, application with peers.

Unit II (6 Hrs)

Design Thinking: definition, need, objective, concepts & brainstorming, stages of design thinking process (explain with examples) – empathize, define, ideate, prototype, test.

Creative Thinking: understanding creative thinking process, understanding problem solving, creative problem solving test.

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the Vaishnay Vidyanee

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^{*}Teacher Assessment shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.



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(2021-2025)

		(202	1 2020	,							
				TEA	CHING	&EVALU.	ATION	SCHE	ME		
			Т	HEORY		PRACT	ICAL				
COURSE CODE	CATEG	COURSE NAME	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	Т	P	CREDITS
BTME510	AESE	DESIGN THINKING AND INNOVATION	60	20	20	0	0	2	0	0	2

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit; *Teacher Assessment shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Unit III (6 Hrs)

Product Design: process of engineering product design, design thinking approach, stages of product design, examples of best product designs and functions, assignment – engineering product design. Prototyping: What is prototype? Why prototype? Rapid prototype development process, testing, sample example, test group marketing

Unit IV (6 Hrs)

Celebrating the Difference: understanding individual differences & uniqueness, group discussion and activities to encourage the understanding, acceptance and appreciation of individual differences Customer Centricity: practical examples of customer challenges, use of design thinking to enhance customer experience, parameters of product experience, alignment of customer expectations with product design.

Unit V (6 Hrs)

Feedback, Re-design & Re-create: feedback loop, focus on user experience, address "ergonomic challenges, user focused design, rapid prototyping & testing, final product, final presentation – "solving practical engineering problem through innovative product design & creative solution".

Text and Reference Books:

- 1. E. Balaguruswamy "Developing Thinking Skills (The way to Success)" Khanna Book Publishing Company, 2022.
- 2. Gavin Ambrose and Paul Harris "Basics Design 08: Design Thinking" Bloomsbury Publishing India Pvt. Ltd. 2009.
- 3. Vijay Kumar "101 Design Methods: A Structured Approach for Driving Innovation in Your Organization" Wiley Pub. 2012.
- 4. Idris Mootee, "Design Thinking for Strategic Innovation: What They Can't Teach You at Business or Design School", John Wiley & Sons 2013.
- 5. Hasso Plattner, Christoph Meinel and Larry Leifer (eds), "Design Thinking: Understand Improve Apply", Springer, 2011
- 6. Roger Martin, "The Design of Business: Why Design Thinking is the Next Competitive Advantage", Harvard Business Press, 2009.

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(2021-2025)

COURSE CATEGORY	08			TI	EACHIN	G &EVAL	UATION	SCHE	EME		
		Т	HEORY		PRAC	ΓICAL					
	CATEGORY	COURSE NAME	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	т	P	CREDITS
BTEC 507	DCC	Programming in Python	0	0	0	30	20	0	0	2	1

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit; *Teacher Assessment shall be based following components: Quiz/Assignment/ Project/Participation in Class, given that no component shall exceed more than 10 marks.

Course Objective:

- 1. Learn Syntax and Semantics and create Functions in Python.
- 2. Handle Strings and Files in Python.
- 3. Understand Lists, Dictionaries and Regular expressions in Python.
- 4. Implement Object Oriented Programming concepts in Python.

Course Outcome:

After learning the course, the student will be able:

- 1. To develop proficiency in creating applications using the Python Programming Language.
- 2. To be able to understand the various data structures available in Python programming language and apply them in solving computational problems.
- 3. To be able to do testing and debugging of code written in Python.
- 4. To be able to draw various kinds of plots using PyLab.
- 5. To be able to do text filtering in Python.

Syllabus

UNIT I

Introduction: History of Python, Need of Python Programming, Running Python Scripts, Variables, Assignment, Operators and Expressions: Operators- Arithmetic Operators, Comparison (Relational) Operators, Assignment Operators, Logical Operators, Bitwise Operators, Membership Operators, Identity Operators, Expressions and order of evaluations.

UNIT II

Data Structures: Lists, Tuples, Sets, Dictionaries, Sequences.

Control Flow - if, if-elif-else, for, while, break, continue. Functions - Defining Functions, Calling Functions, Passing Arguments. Modules: Creating modules. import statement, from, import statement, name spacing.

UNIT III

Python packages, Introduction to PIP, Installing Packages via PIP, Using Python Packages

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				TI	EACHIN	G &EVAL	UATION	SCH	EME		
COURSE CATEGORY		Т	HEORY		PRAC	ΓICAL					
	CATEGORY	CATEGORY COURSE NAME	END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	LT	P	CREDITS
BTEC 507	DCC	Programming in Python	0	0	0	30	20	0	0	2	1

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UNIT IV

Object Oriented Programming OOP in Python: Classes, 'self variable', Methods, Constructor Method, Inheritance, Overriding Methods, Data Hiding.

UNIT V

File Handling: Types of Files, Creating and Reading Text Data, File Methods to Read and Write Data.

List of Experiments:

- 1. Develop programs to understand the control structures of python.
- 2. Develop programs to learn different types of structures (list, dictionary, tuples) in python.
- 3. Write a Python program to sum all the items in a list.
- 4. Write a Python program to get the largest and smallest number from a list.
- 5. Develop programs for data structure algorithms using python searching and sorting.
- Write a Python Program to perform Linear Search.
- 7. Write a Python Program to perform Binary Search.
- 8. Write a Python Program to perform Selection sort.
- 9. Write a Python Program to perform Insertion sort.
- 10. Write a Python Program to perform Merge sort.
- 11. Write a Python program to get a list, sorted in increasing order by the last element in each tuple from a given list of non-empty tuples: Sample List: [(2, 5), (1, 2), (4, 4), (2, 3), (2, 1)] Expected Result: [(2, 1), (1, 2), (2, 3), (4, 4), (2, 5)]
- 12. Write a Python program to check a list is empty or not.
- 13. Write a Python program to remove duplicates from a list.
- 14. Programs that take command line arguments (word count).
- 15. Write a Program that Reads a Text File and Counts the Number of Times a Certain Letter Appears in the Text File.
- 16. Write a Program to Read a Text File and Print all the Numbers Present in the Text File.

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(2021-2025)

COURSE CODE	CATEGORY	COURSE NAME	TEACHING &EVALUATION SCHEME								
			THEORY			PRACTICAL					
			END SEM University Exam	Two Term Exam	Teachers Assessment*	END SEM University Exam	Teachers Assessment*	L	Т	P	CREDITS
BTEC 507	DCC	Programming in Python	0	0	0	30	20	0	0	2	1

Legends: L - Lecture; T - Tutorial/Teacher Guided Student Activity; P - Practical; C - Credit; *Teacher Assessment shall be based following components: Quiz/Assignment/ Project/Participation in

Class, given that no component shall exceed more than 10 marks.

17. Write a Program to find the most frequent words in a text read from a file.

18. Implement Object Oriented Programming concepts in Python.

19. Write A Program to Append, Delete and Display Elements of a List Using Classes.

- 20. Write A Program to Create a Class and Compute the Area and the Perimeter of the Circle.
- 21. Write A Program to Create a Class which Performs Basic Calculator Operations.
- 22. Write A Program to Create a Class in which One Method Accepts a String from the User and another prints it.
- 23. Learn to plot different types of graphs using PyPlot.

References:

- 1. John V Guttag. "Introduction to Computation and Programming Using Python", 3nd edition, Prentice Hall of India, 2021
- 2. Wesley J. Chun. "Core Python Programming" 3rd Edition, Prentice Hall, 2012
- 3. Michael T. Goodrich, Roberto Tamassia, Michael H. Goldwasser, "Data Structures and Algorithms in Python", Wiley, 2013
- 4. Kenneth A. Lambert, "Fundamentals of Python First Programs", CENGAGE Publication, 2nd edition, 2018.

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