Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore (MP)

Choice Based Credit System (CBCS) Scheme

M.Tech. in Embedded System

II - SEMESTER

Sr. No.	Subject Code	Name of Subject	Course Code	Teaching Scheme/ Week			Examination Scheme					Total Marks	Credits
							Theory			Practical			
				L	T	P	End Sem Unversity Exam	Two Term Exam	Teachers Asses-ment*	End Sem Unversity Exam	Teachers Asses-ment*		
1	MTES201	Advance Controllers		3	1	2	60	20	20	30	20	150	5
2	MTES202	Embedded Operating System		3	1	2	60	20	20	30	20	150	5
3	MTES203	FPGA Architecture & Applications		3	1	2	60	20	20	30	20	150	5
4	MTDC124 /MTDC214	Elective: 1 CMOS VLSI Design 2 Cryptography & E-Security		3	1	0	60	20	20	0	0	100	4
5	MTES215 /MTES225	Elective: 1 Embedded Control System Design 2 Communication Protocols & Interface		3	1	2	60	20	20	30	20	150	5
6	MTES206	Comprehensive Viva		0	0	0	0	0	0	0	50	50	4
7	MTES207	Seminar		0	0	4	0	0	0	0	50	50	2
TOTAL				15	5	12	300	100	100	120	180	800	30

*Teacher Assessment shall be based on following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.

Chairperson
Board of Studies
Shri Vaishnav Vidyapeeth Vishwavidyalaya
Indore

Registrar
Shri Vaishnav Vidyapeeth Vishwavidyalaya
INDORE (M.P.)