Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore (MP)

Choice Based Credit System (CBCS) Scheme

M.Tech. in Embedded System

I - SEMESTER

Sr. No.	Subject Code	Name of Subject	Course Code	Teaching Scheme/ Week			Examination Scheme					Total Marks	Credits
							Theory			Practical			
				L	T	P	End Sem University Exam	Two Term Exam	Teachers Asses-ment*	End Sem University Exam	Teachers Asses-ment*		
1	MTMA101	Advance Mathematics		3	1	0	60	20	20	0	0	100	4
2	MTES101	Introduction to Embedded System		3	1	0	60	20	20	0	0	100	4
3	MTES102	Microcontrollers & Interfacing		3	1	2	60	20	20	30	20	150	5
4	MTES113/ MTES123	Elective: 1 HDL Fundamentals 2 Data Acquisition & Signal Conditioning		3	1	2	60	20	20	30	20	150	5
5	MTDC202 /MTES114	Elective: 1 Modern Digital Signal Processing 2 Wireless Sensor Networks		3	1	2	60	20	20	30	20	150	5
6	MTDC105	Linux & C Programming		0	0	2	0	0	0	30	20	50	1
7	MTES106	Comprehensive Viva		0	0	0	0	0	0	0	50	50	4
8	MTES107	Seminar		0	0	4	0	0	0	0	50	50	2
TOTAL				15	5	12	300	100	100	120	180	800	30

***Teacher Assessment shall be based on following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.**

Chairperson
Board of Studies
Shri Vaishnav Vidyapeeth Vishwavidyalaya
Indore

Registrar
Shri Vaishnav Vidyapeeth Vishwavidyalaya
INDORE (M.P.)